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J. R. Hughes[a]; E. P. Raynes[ab]
[a] Defence Research Agency (Malvern), Worcestershire, England [b] Sharp Laboratories of Europe Ltd., Oxford, England

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A new set of high speed matrix addressing schemes for ferroelectric liquid crystal displays

by J. R. HUGHES and E. P. RAYNES*†

Defence Research Agency (Malvern), St. Andrew's Road, Malvern, Worcestershire WR14 3PS, England

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A new set of matrix addressing schemes for ferroelectric liquid crystal displays is reported. The schemes use the minimum in the response time–voltage characteristic found in certain mixtures and deliver improved operating speed and contrast ratio compared with previously reported schemes operating in this mode.

The electrooptic effect in thin layers of ferroelectric smectic C materials [1, 2] is fast and bistable, thus providing a route to high information content displays which overcomes the limitations of root mean square (r.m.s.) addressed displays such as supertwist nematic liquid crystal displays (STN LCDs) without the fabrication complexities of thin film transistors (TFT's). No optimum drive scheme has been devised for ferroelectric liquid crystal displays (FLCDs) although there are many in the literature (see, for example [3]). Drive schemes fall into two categories, those designed to work with materials having a conventional response time–voltage characteristic (τ–V constant) and those showing a minimum in their switching characteristic (τ–V minimum) [4, 5]. These characteristics are illustrated in figure 1. The 'τ–Vmin' mode of operation has been shown to give fast switching speeds, high contrast and a wide operating range [3, 6].

One of the best known drive schemes used in the τ–V minimum mode is the JOERS/Alvey scheme [3], illustrated in figure 2. The benefits of this mode of operation accrue largely from the good discrimination achieved between the high voltage resultant pulse, $|V_s + V_d|$, and the low voltage resultant pulse, $|V_s - V_d|$. In the τ–V minimum mode, switching is effected by the low voltage resultant pulse, $|V_s - V_d|$, and not the high voltage resultant pulse $|V_s + V_d|$, as shown in figure 3. Good discrimination is difficult to achieve in τ–V constant drive schemes.

In order to induce a minimum in the τ–V characteristic it is necessary to have a modest value of P_s to balance the dielectric restoring torque [7]. This would lead to a reduced switching speed with conventional schemes, but fast switching speeds are still obtained with τ–V minimum schemes because the switching characteristic is modified by the pulse immediately preceding the resultants $|V_s - V_d|$ and $|V_s + V_d|$, giving two separate τ–V characteristics (see figure 3). The curve on which the device switches is much lower (faster) than the characteristic measured with a simple mono-strobe. It is these two modified curves which must be taken into consideration when considering

* Author for correspondence.

† Present address: Sharp Laboratories of Europe Ltd., Edmund Halley Road, Oxford Science Park, Oxford OX4 4GA, England.

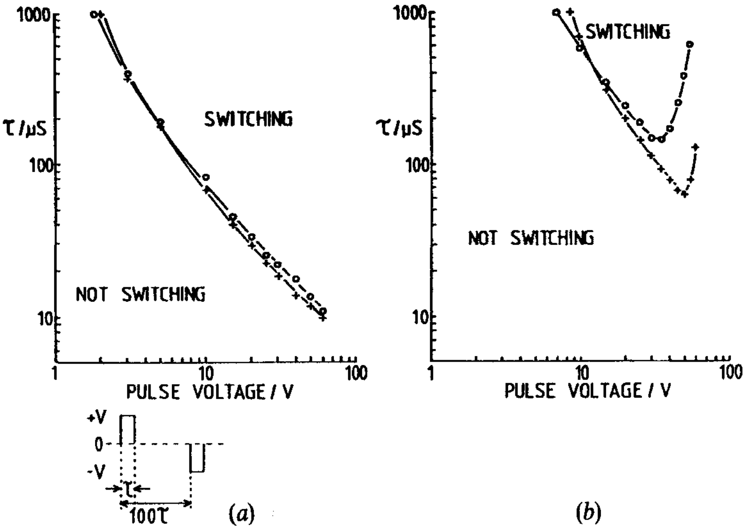

Figure 1. Response time as a function of voltage required to switch the device between states using a simple mono-pulse with a superimposed AC bias (50 kHz square wave) to simulate the effect of column voltages encountered during matrix addressing. (*a*) τ–V constant: material SCE12 (E. Merck Ltd.), with OV r.m.s. AC bias (+), 7·5 V r.m.s. AC bias (○). (*b*) τ–V minimum: material SCE 8 (E. Merck Ltd.), with O V r.m.s. AC bias (+), 10 V r.m.s. AC bias (○).

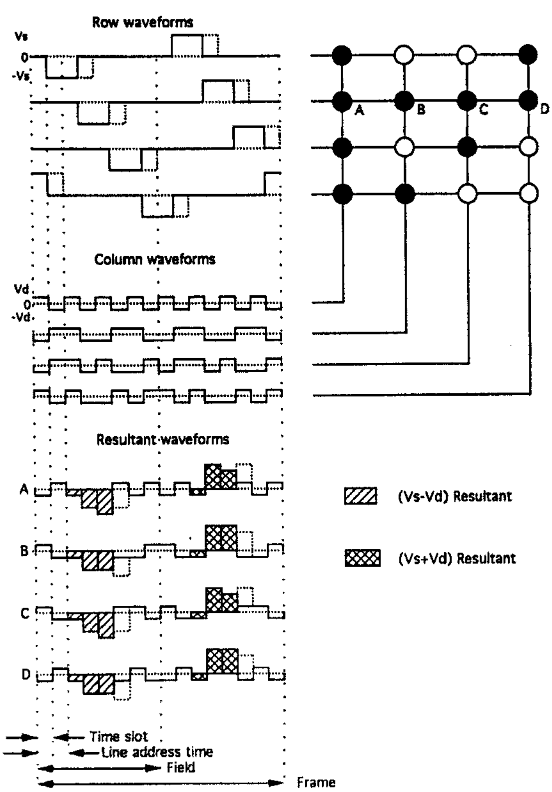

Figure 2. Simple example of the JOERS/Alvey drive scheme for the case of four way multiplexing. When operating in the τ–V minimum mode, the switch pulse will be $(V_s - V_d)$ and pulses of amplitude $(V_s + V_d)$ and V_d will not switch. Pixel A is arbitrarily defined to be 'off' in response to a $-(V_s - V_d)$ pulse.

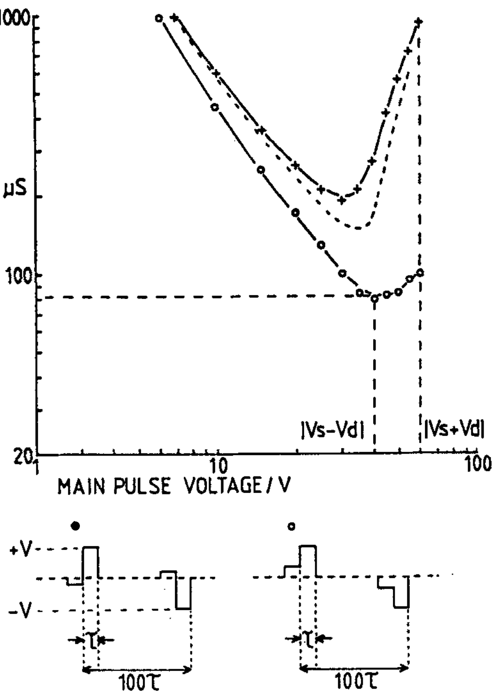

Figure 3. Response time as a function of voltage required to switch the device between states for the material SCE 8, simulating the resultant pulses encountered in the JOERS/Alvey addressing scheme under conditions of $V_s = 50V$, $V_d = 10V$. The curves relate to the $(V_s + V_d)$ resultant pulse (+) which has a leading part of opposite polarity and amplitude 0·166 of the main pulse, and the $(V_s - V_d)$ resultant pulse (○) which has a leading part of the same polarity and amplitude 0·25 of the main pulse. The broken line shows the response measured with a monopolar pulse as illustrated in figure 1 (*b*). The operating voltages are denoted by vertical lines and the fastest operating point by a horizontal line.

discrimination during matrix addressing, rather than the simple characteristics of figure 1.

A new set of matrix addressing waveforms is presented here which operates in the τ–V minimum mode. In this new set of waveforms the strobe pulse is extended from the line address period into following time slots so that switching takes place over more than one line address period. This is illustrated in figure 4. The apparent, two time slot, line address period may now be reduced in width to compensate for the lengthened switching pulse. A family of drive schemes is obtained, since the pulse extension may be over more than one slot, as illustrated. We term this family of drive schemes the 'Malvern schemes' and identify the scheme by the number of slots width of the strobe pulse, hence 'Malvern-2', etc.

Some complications arise because the effective prepulse is reduced from a width equal to the switching pulse in the JOERS/Alvey scheme to some fraction (one-half or less) of it and this reduces the discrimination between switching and non-switching pulses. Secondly, the trailing part of the pulse is modulated by the column data waveform in following line address periods, and this may be of either phase and thus randomly enhances or detracts from switching. Nevertheless a significant increase in speed is obtained at the cost of a reduction in operating pulse width range, and since

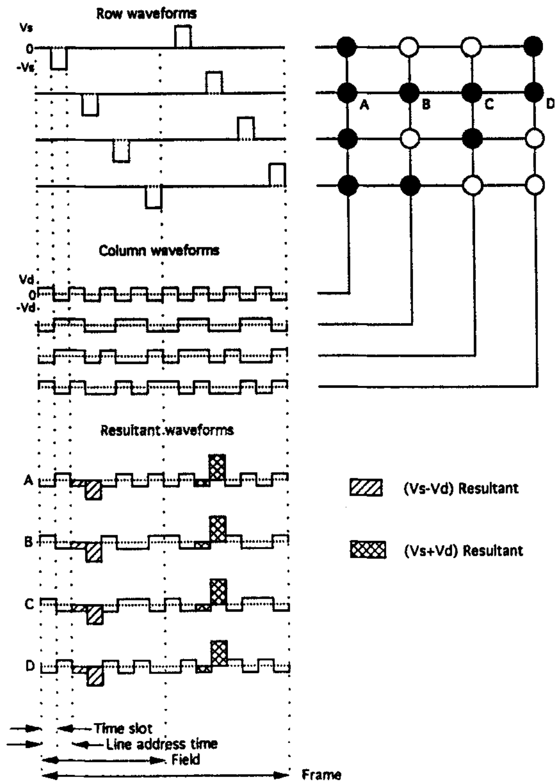

Figure 4. Simple example of the Malvern-2 (solid line) and Malvern-3 (dotted line) drive schemes for the case of four way multiplexing. When operating in the τ–V minimum mode, the switching pulse will be $(V_s - V_d)$ and pulses of amplitude $(V_s + V_d)$ and V_d will not switch. Pixel A is arbitrarily defined to be 'off' in response to a $-(V_s - V_d)$ resultant pulse.

this reduction occurs at the long pulse width region of the operating range, it is not considered to be too detrimental.

Measurements have been made on single pixel test devices of nominal 1·8 μm thickness with aligning layers of rubbed polymer. Good alignment was achieved by cooling from the pseudo nematic phase through a smectic A phase into the smectic C phase [8]. The cells were held in a temperature controlled stage which was mounted on a polarizing microscope. Resultant matrix addressing waveforms representative of those which would be encountered by a single pixel in a matrix device were calculated on a Hewlett–Packard 300 series computer and loaded into an arbitrary waveform generator from where they were amplified and fed to the cell. Transmission was measured with a Si photodiode fitted with a photopic eye-response filter.

The fastest line address time (l.a.t.) was measured as that at which switching took place within one frame of the matrix addressing waveform; the longest line address time was that at which the non-switching pulse began to cause partial switching, visible as speckle patches in the device. The operation range is the ratio of these two line address times. The contrast ratio was measured at the fastest line address time.

Results are given in the table which shows a number of interesting features. The Malvern schemes deliver operation speed and contrast ratio which are superior to these from the JOERS/Alvey scheme at the cost of a reduced operation range in line address time. The speed improvement is not always in direct proportion to the extended

Comparison of performance of JOERS/Alvey (J/A), Malvern-2 (M-2) and Malvern-3 (M-3) drive schemes. Measurements made at 25°C.

	J/A	M-2	M-3
(i) Material ZLI 5014-000 (E. Merck.)			
Matrix addressing voltages $V_s = 50\,V$, $V_d = 10\,V$			
Line address time (l.a.t.) μs	72	36	30
Operating range (maximum/minimum l.a.t.)	3·9	2·3	1·7
Contrast ratio (at minimum l.a.t.)	23	50	47
(ii) Material SCE 8 (Merck Ltd.)			
Matrix addressing voltages $V_s = 40\,V$, $V_d = 7{\cdot}5\,V$			
Line address time (l.a.t.) μs	190	92	68
Operating range (maximum/minimum l.a.t.)	3·6	1·9	1·7
Contrast ratio (at minimum l.a.t.)	49	77	64
(iii) Material A (difluoroterphenyl host with a P_s of $6{\cdot}7\,nC\,cm^{-2}$)			
Matrix addressing voltages $V_s = 40\,V$, $V_d = 10\,V$			
Line address time (l.a.t) μs	112	78	66
Operating range (maximum/minimum l.a.t.)	2·7	2·5	2·6
Contrast ratio (at minimum l.a.t.)	32	46	48

switching pulse width and can be affected by the pixel pattern on the display. These features will be covered in a further communication on these new drive schemes.

A new family of FLCD drive schemes has been described which combine the virtues of the 'τ–Vmin' mode of operation, such as wide operating range and good contrast with improved switching speed. This opens the possibility of improved temporal grey scale and colour performance, greater complexity at video rates, or some combination of these benefits.

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